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FAILURE MECHANISMS OF GaAs TRANSISTORS - A LITERATURE SURVEY

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13. ABSTRACT (Maximum 200 words)

This report is a summary of information from a literature survey of GaAs component failure modes. A brief outlook on GaAs material and techniques used in fabrication of GaAs devices is included. Failure modes common to GaAs MESFET's are discussed excluding modes common to Si components such as metal migration and intermetallic formation. As the same failure modes seen in discrete MESFET's will occur in MMIC and digital GaAs devices, the discussion does not include these devices per se. Sidegating or backgating problems seem to be material or design related and therefore are not treated as failure modes. Besides the interaction of metal and GaAs in ohmic contact areas, the importance of the quality of the GaAs surface in the reliability of GaAs components is discussed. Also discussed is the relation of free As on the surface to both long and short term failure modes.

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EVALUATION

This technical report, although not inclusive in its treatment of GaAs device reliability, provides a good introduction to failure modes unique to GaAs devices as reported in the MESFET literature. The report includes a brief overview of GaAs material and techniques used in fabrication of devices. The topics discussed include: importance of the metallization system used to device reliability, interaction of metal and GaAs in ohmic contact areas, effect of outdiffusing of Ga and indiffusing of gold at ohmic areas on the stoichiometry of near surface volumes and device performance, the importance of the quality of the GaAs surface to device reliability, and the effect of free As, at the surface, on long and short term failure modes.

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1.0 INTRODUCTION

This report is a summary of information from a literature survey of GaAs components failure modes. A brief outlook of GaAs material and techniques used in fabrication of devices are included. The failure modes discussed are concentrated on GaAs MESFET's, excluding modes known from Si components such as metal migration and intermetallic formation. As the same failure modes seen in discrete MESFET's will show up in MMIC and digital devices, no discussion is carried out for these devices per se. Sidegating or backgating problems seem to be material or design related and is not treated as failure modes.

Beside interacting of metal and GaAs in ohmic and Schottky contact areas, the quality of the GaAs surface seems to be of great importance for the reliability of components. Outdiffusing of Ga and indiffusing of gold at ohmic areas may, for instance, alter the stoichiometry of near surface volumes and change the performance of a device.

The surface of semiconductors represent locations where the lattice of atoms is discontinuous and the physics of these surfaces is very complex. For Si semiconductors, the native oxide SiO_2 is acting enough like Si to passivate the surface, no equivalent dielectric layer has been found to similarly passivate GaAs, the numerous surface defects are therefore creating a large number of surface states. Free As on the surface seems to be one of the main reasons for both long and short term failure modes. A clean surface wihtout native oxides of Ga and specially not As, which react with GaAs to form free As, and with correct stoichiometry is needed for high reliability components. The metallization system used is also of great importance for the reliability of the components.

2.0 GaAs MATERIAL

Gallium arsenide is a III-V compound semiconductor. It is composed of an element (Ga) from column III of the periodic chart and an element (As) from column V. The crystalline structure is formed by carefully alternating Ga and As atoms in a precise 1 to 1 sequence.

Gallium is relatively easy to handle. The melting point is 30°C and the boiling point 2403°C. GaAs crystals are grown from a melt at 1240°C, far below the boiling point of Ga. Purifying Ga, on the other hand, is extremely difficult, and the price for pure grades is high. An idea of the difficulty is the fact that only a few parts per million of zinc or copper, which dissolves very easily in liquid gallium, can affect the final electronic circuit performance.

Arsenic is quite different due to its high vapor pressure, which reaches 1 atm at 611°C where it sublimes. The As vapor pressure over melted GaAs at the melting point 1240°C is 0.976 atm. Unless preventive measures are taken, a GaAs melt will become Ga rich as it loses As. To grow GaAs crystals of good quality, the Ga to As ratio must be between 1.00 and 1.04. Arsenic is easily contaminated with traces of carbon, iron and silicon during processing.

The chemical reaction between Ga and As proceeds rapidly and exothermically above 800°C. GaAs is grown in crystal ingots from which individual wafers are sawed, lapped and polished. There are two principal methods of growing GaAs bulk crystals:

- Horizontal Bridgman (HB)
- Liquid Encapsulated Czochralski (LEC)

The following description gives the principles of the methods, actual processing methods may be different as both methods have numerous variations.

2.1 HORIZONTAL BRIDGMAN

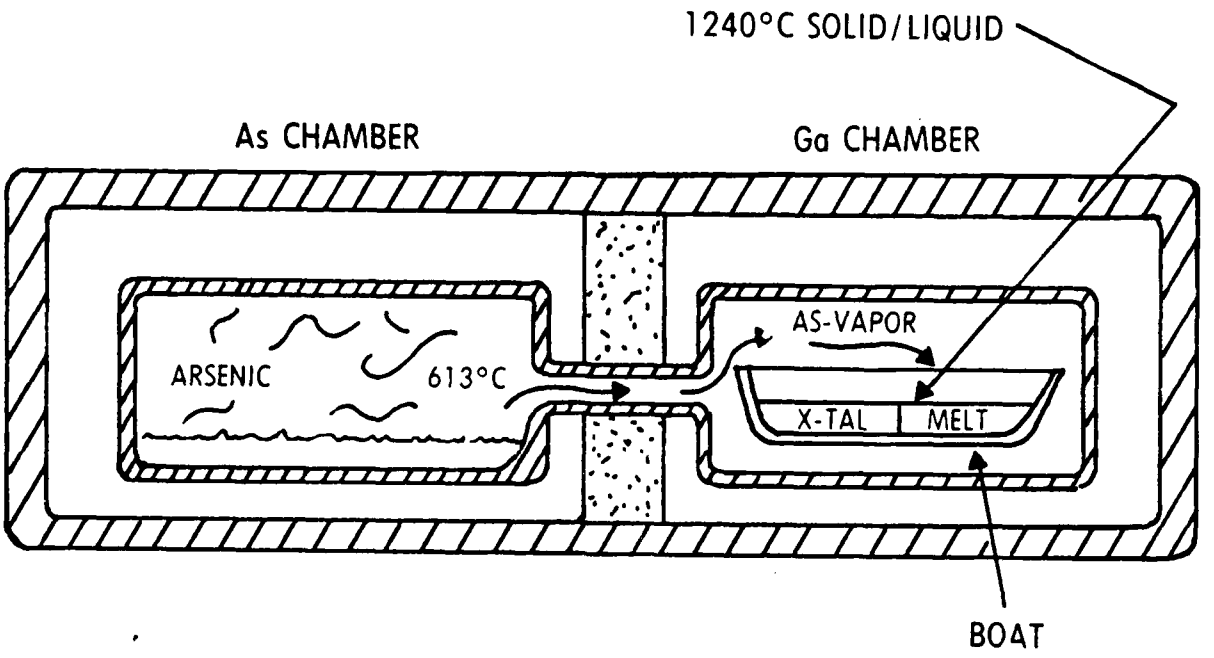

Fig 2.1 Horizontal Bridgman (HB) Method for Growing GaAs Crystals

In the HB method Ga and As are placed in separate evacuated and sealed ampoules, backfilled with an inert gas, connected by a passageway to allow transport of arsenic vapor. The Ga chamber is heated to slightly above the melting point of GaAs and the As chamber is heated to 613^{o}C. Arsenic evaporates and travels into the Ga chamber where it reacts with the Ga. Once the melt is formed, a solid liquid interface is moved along the quartz boat. The quartz boat is a primary source of Si impurity in HB grown GaAs. Crystal growth is usually chosen to be in the (111) direction. The complete crystal has a cross-sectional shape matching the shape of the boat: somewhat circular up to the level of the melt. HB crystals are usually sawed at an angle of 54.7^{o} to the ingot axis to get (100) slices which are desired for epitaxial growth.

2.2 LIQUID ENCAPSULATED CZOCHRALSKI (LEC)

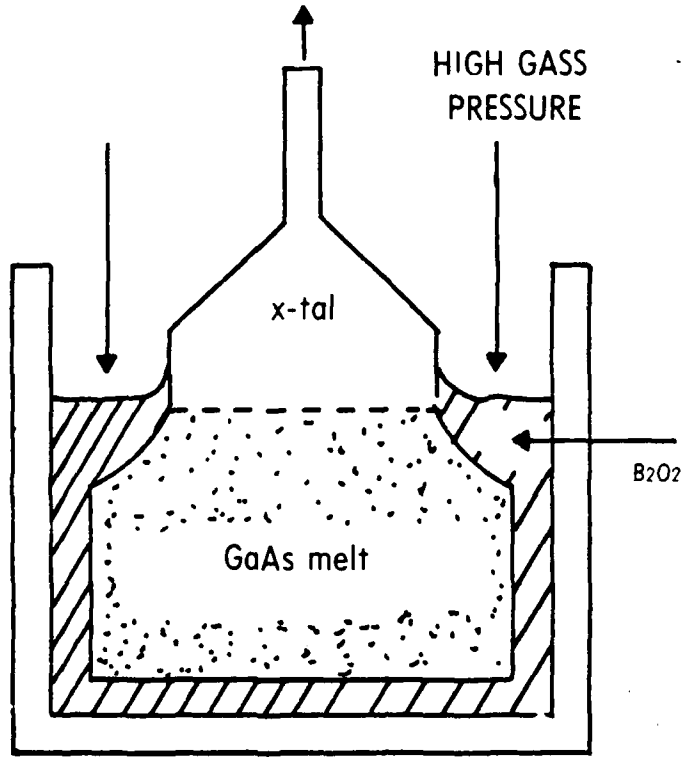

Fig 2.2 Liquid Encapsulated Czochralski (LEC) Growth of GaAs Crystal

In the liquid encapsulated Czochralski (LEC) process the crystal is grown in the vertical direction by slowly pulling the ingot from a melt, consisting of molten GaAs protected by a layer of liquid boric oxide (B_2O_2). A GaAs seed crystal is used to begin the process when appropriate temperature profiles are present.

Bulk GaAs cannot be prepared in truly pure form but is polluted during the fabrication process. Silicon is available from the quartz parts used in bulk growth, carbon is available from graphite heaters and may be transported in gaseous compounds. The ability to grow semi-insulating GaAs depends on complex compensation methods, for instance chromium may be intentionally added to the melt to compensate for silicon impurities.

In general, LEC material exhibits a greater dislocation density than HB material, this

is its major disadvantage compared to HB. Dislocation density depends strongly on the size of the ingot being grown and can easily be 10^4 to 10^5 dislocations/cm^{-2} for 2-inch and 3-inch material. Comparable HB material generally exhibits dislocation densities ranging from 8000 to 25,000 cm^{-2}. Dislocations generally arise from temperature gradients present during crystal growth.

2.3 PHYSICAL AND ELECTRICAL CHARACTERISTICS

Fig 2.3 shows band diagrams for GaAs and Si crystals, the energy bands are functions of the magnitude of the electron momentum k.

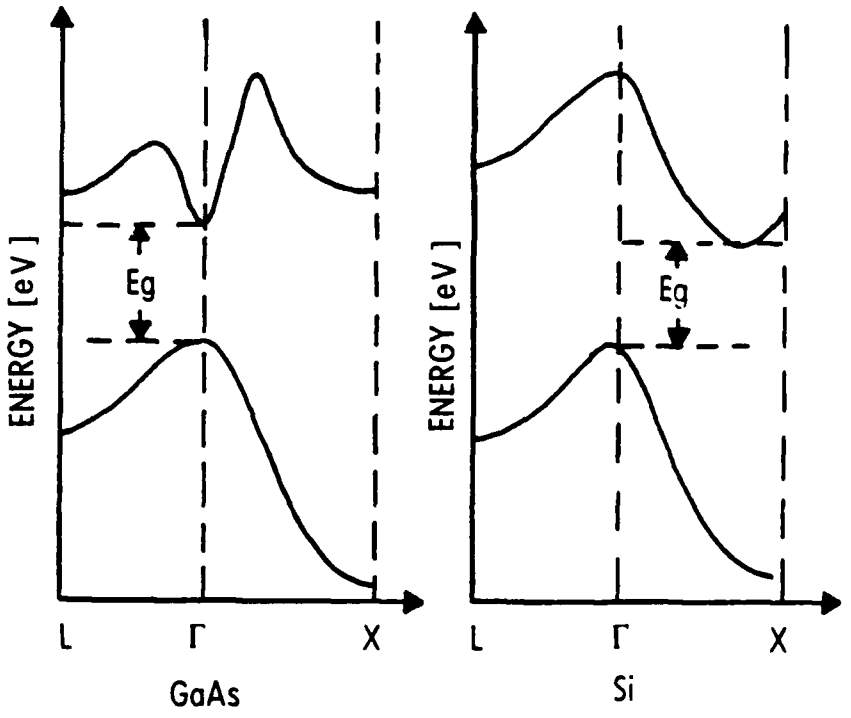

Figure 2.3 Energy Band Diagram of GaAs and Si

Transistions between bands generally involve movement from an energy state near the maximum of the valence band to an energy state near the minimum of the conduction band. GaAs is a direct bandgap semiconductor; that means a transition only requires a change in energy. Electrons can make the transistion by absorbing or

emitting energy quanta.

Silicon is an indirect bandgap semiconductor in that the minimum and maximum of the two bands are at different momenta. For an electron to make a transistion it is necessary to change momentum as well as energy. The change of momentum is possible if the electron interacts with the lattice. This is less likely to occur, thus indirect semiconductors are not as suitable for optical devices as direct bandgap semiconductors.

The energy band structure described assumes a pure semiconductor and a crystal without defects or surfaces. Any departure from this, such as the presence of crystal defects, surfaces or dopant atoms changes the energy band structure near the inhomogeneity. Figure 2.4 shows deep levels signature of electron traps observed by Deep-Level Transient Spectroscopy (DLTS). EL 2 typically predominates, it is a donor level at 0.8eV.

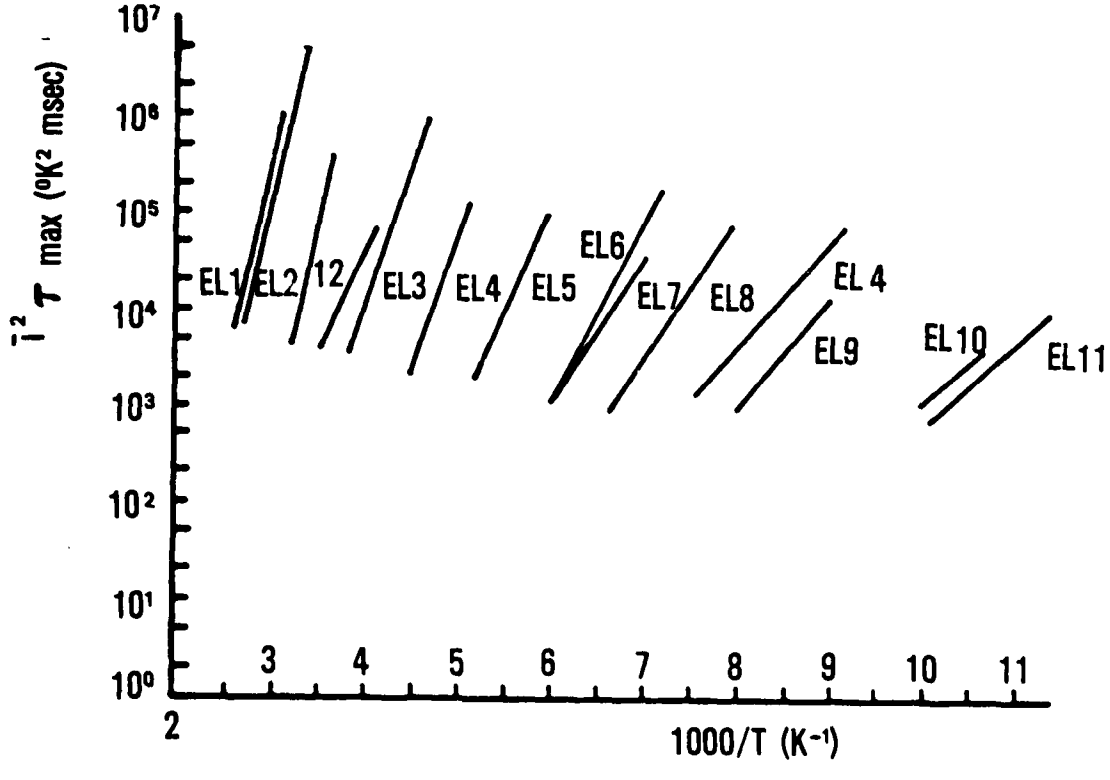

Figure 2.4 Deep Levels DLTS Signature of Electron Traps. (Ref 1)

Some of the properties of GaAs and Si are shown in Table 2.1

ROOM TEMPERATURE (300°K) PROPERTIES

	GaAs	Si	
Lattice Constant	5.65		A
Density	5.32		g/cm^3
Atomic Density	$4.43X10^{22}$		$atoms/cm^3$
Molecular Weight	144.6		
Bulk Modulus	$7.55X10^6$		N/cm^2
Sheer Modulus	$7.26X10^6$		N/cm^2
Linear exp. coeff.	$5.73X10^{-6}$		K^{-1}
Spec Heat	0.327		J/g-K
Lattice Thermal Cond.	0.55	1.5	W/cm-K
Dielctr. Const	12.85		
Bandgap	1.423	1.12	eV
Threshold Field	$3.3X10^3$		V/cm
Peak Drift Velocity	$2.1X10^7$		cm/s
Electron Mobility (undoped)	8500	1500	$cm^2/V-s$
Hole mobility (undoped)	400	600	$cm^2/V-s$
Melting point	1238		°C
Minority Carrier Lifetime	10^{-8}	$2.5X10^{-3}$	s
Vapor Pressure	10^2 at 1220°C	10^{-3} @ 1600 °C Torr	
	1 at 1050°C	10^{-8} @ 930 °C Torr	

TABLE 2.1 PROPERITIES OF GaAs and Si

2.4 WAFER MATERIALS

Due to the large energy bandgap GaAs offers bulk semi-insulating substrates. The theoretical intrinsic resistivity is as high as $4X10^8$ ohm-cm, the resistivity of real life substrates may be on the order of 10^7 ohm-cm. Devices can thus be isolated without an additional implant. A parameter which dictates the temperature limitations of the processing technology is the vapor pressure of the material. The vapor pressure in GaAs is so high that the material begins to decompose at temperatures as low as 500^0C. This obviously destroys the stoichiometry of the compound.

Decomposition during high-temperature processing can be prevented by capping the wafer with a dielectric such as SiO_2 or Si_3N_4 to seal in the As and preserve the stoichiometry, or arsenic overpressure can be used for the same purpose. In contrast Si processing can employ temperatures as high as 1200^oC without adverse reactions.

GaAs substrates can be produced with p-type doping densities ranging from 10^{17} to 10^{19} atoms/cm^2 and n-type doping as high as 10^{18} atoms/cm^3. Doping of Si substrates is a much more understood process and the doping densities for both n- and p-tye can be controlled between 10^{14} and 10^{20} atoms/cm^3. The background doping from impurities from quartz utensils used during the GaAs growth process are n-type due to Si atoms and can range from 10^{15} to 10^{17} atoms/cm^3. Si acts as a shallow electron donor about 0.002 eV below the conduction band edge, these free carriers can be compensated for by the addition of chromium (Cr) during crystal growth. Cr acts as deep electron traps located 0.7eV above the valence band edge. If enough Cr is added, the resistivity of the material can be about 10^7 ohm-cm.

GaAs is very brittle, therefore the wafers have to be thicker than their Si counterparts to avoid handling problems during fabrication processes.

To be useful, active layers must be formed in or on the substrate. This can be

achieved by ion implantation, diffusion or epitaxial growth.

2.5 EPITAXY

An epitaxy layer is formed by growing an additional GaAs layer on the surface of a GaAs substrate in a manner that preserves the crystal structure, dopants may be included. Epitaxial layers are generally of higher crystal quality than the substrate they are grown on. Crystal defects from the substrate usually heals out when the epitaxy grows thicker. Therefore a buffer layer of undoped GaAs often is grown on the substrate first, then a thin (a few tenths of a micron) active layer with doping is grown and in some cases a top layer of highly doped material may be grown to provide a contact layer. These three layers (buffer, active and contact) are sometimes referred to as n_o, n and n^+ layers.

There are three basic types of epitaxy that is used for GaAs:

Liquid Phase Epitaxy (LPE)

Vapor Phase Epitaxy (VPE)

Molecular Beam Epitaxy (MBE)

RBRE has its own MBE system, therefore only the MBE epitaxy will be described here (Ref 2). A description of the two other systems may be found in any textbook.

Molecular beam epitaxy (MBE) may be described as a sophisticated evaporation technique performed in ultrahigh vacuum. In this procedure, the substrate is placed in a high vacuum where elemental species are evaporated from ovens, and impinge upon the heated substrate. Here they assemble into crystalline order. With proper control of the sources (Ga, As, Al, Si, etc) almost any material composition and doping can be achieved. Further, the composition may be controlled with a resolution of virtually one atomic layer. Figure 2.5 shows a schematic view of the growth chamber of an MBE machine. The separate ovens, often called effusion cells, each contain an individual element. The heated materials vaporize and exit the effusion

cell through one end, go past a shutter, and travel through the growth chamber until reaching the substrate. The substrate is heated to provide sufficient energy for surface diffusion and incorporation of the species. This temperature is typically 500° to 600°C for GaAs. The slice usually is rotated to aid uniformity. Elements may be switched on and off using the shutter in front of each effusion cell.

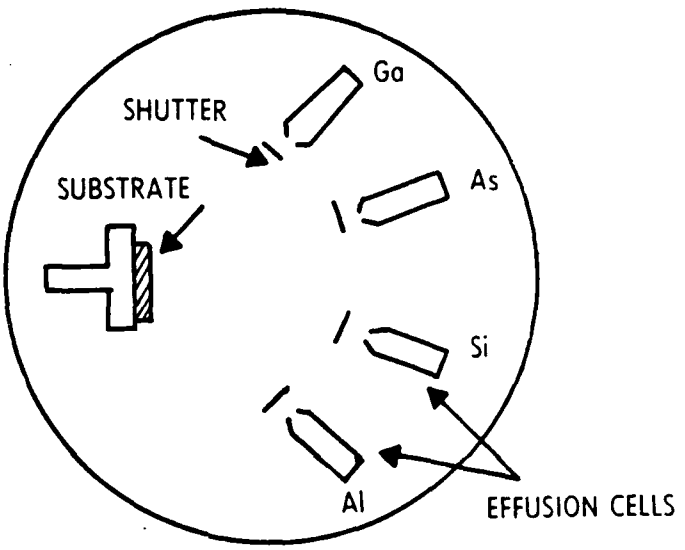

Figure 2.5 Schematic Diagram of a MBE System

MBE's advantages are that it can produce almost any epitaxial layer composition, layer thickness, and doping; and it can do so with high accuracy and uniformity across a slice. Disadvantages include high vacuum requirements, complex and costly equipment, and slow growth rate. An ultrahigh vacuum is required in the growth chamber, generally in the range 10^{-10} to 10^{-11} Torr. This is an exceedingly difficult requirement, especially in the presence of heated substrates and heated

effusion ovens. Growth rate is typically 1 um/hour (about one atomic layer per second) although growth rates up to 10 um/hour may be attainable.

MBE machines usually incorporate instruments to analyze the growth process and the resulting crystal structure, the RBRE machine has an Auger instrument attached.

2.6 ION IMPLANTATION

During ion implantation the dopant atoms are ionized and accelerated by an electric field and reach the substrate surface with a high kinetic energy. After penetrating the surface, they come to rest at random locations within the material. Typical kinetic energies are from 30KeV to 400KeV and implanted doses typically range from 10^{12} to 10^{14} atoms/cm^3. When the atoms hit the material they greatly damage the crystal lattice, a high temperature annealing step is necessary for the lattice damage to recover and to allow the implanted atoms to move into lattice sites. This is known as activating the implant. Not all the dopant atoms are incorporated at lattice sites and supply carriers, activation is generally in the range of 75% to 95% and depends on the implant and anneal conditions.

Ion implantation can be performed with high uniformity over a wafer and with good uniformity from wafer to wafer. Doping by ion implantation can be performed locally by selectively masking the substrate; this makes it possible to use different doping levels on the same slice. Monolithic low noise amplifiers may for instance need high doping (low noise) for input transistors and medium doping (high power) for output transistors.

Ion implantation is performed at a slight angle to the surface of the substrate on the order of 6° to 10°. This is done to avoid channeling. If the crystal lattice is viewed in an appropriate direction, there are open cells or channels which contain no atoms. An ion moving parallel to a channeling direction can travel deep into the crystal before scattering occurs.

There are two mechanisms responsible for energy loss of the ions as they enter the substrate and come to rest. The first is elastic scattering from the nuclei of the substrate atoms, nearly all the angular deviation is caused by nuclear scattering. The second is inelastic interactions between the ions and the electrons of the substrate, this acts as viscous damping and contributes little to the angular deviations.

The substrate may be implanted at room temperature or it may be heated. The doping profile cannot be as sharp as with epitaxial methods. This is the result of the statistics of the implantation and the general diffusion that takes place during high temperature anneal. Implanted atoms scatter off the atoms of the host crystal and come to rest in a near Gaussian distribution by the depth, the tail of the curve extends deeper than a true Gaussian. A second, shallower implant is sometimes used to fill in the area near the surface and make the doping profile more uniform.

Annealing usually takes place in high temperature ovens between 800°C and 900°C. At these temperatures, the crystal tends to decompose and emit arsenic. To keep the arsenic from leaving the crystal arsenic overpressure or an encapsulant can be used on the wafer. The encapsulant method seems to be the most used. Silicon dioxide or silicon nitride is used as encapsulant and grown on the substrate before ion implantation. The implantation can be performed directly through the encapsulating layer which then remains on the slice during annealing. Problems related to deficiencies in the GaAs materials present problems for LSI components fabricated in a cost-affordable way. These problems are related to primary defects associated with the crystal growth process and secondary defects related to wafer preparation. Significant efforts have been directed towards advancing high pressure LEC growth technology and improving GaAs wafer fabrication techniques during the recent years. These efforts range from improving the purity of elemental Ga and As to development of digital diameter control systems. Orioto et al (Ref 3) reports growth of large size 3 and 4-inch diameter dislocation-free and striation-free GaAs single crystals with high electrical uniformity. They used a vertical magnetic-field-applied fully encapsulated Czochralski technique combined with in-doping.

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2.3 Funi Orito et al, Large Size Dislocation-Free Gallium Arsenide Single Crystals for LSI Applications, GaAs IC Symposium, October 1986, Technical Digest 1986.

3.0 CONTACTS TO GaAs DEVICES

The electrical properties of III-V semiconductor interfaces are determined to first order by native defects (vacancies, antisite defects or more complex defects). The physical defects and their energy levels are independent of which foreign atoms are deposited on the clean surface, but the densities of the defects are not independent of which foreign atom is deposited as chemical interactions between the overlayer and the semiconductor may modify the defect concentration. Due to the high density of electronic states at a few discrete energies at the metal-semiconductor interface the Schottky barrier height on GaAs is insensitive to the choice of metal. But the high density of states also has created device problems as poor ohmic contacts.

3.1 THE UNIFIED DEFECT MODEL FOR III-IV INTERFACES

W. E. Spicer (Ref 1) gives a model of the atomically clean free surface of GaAs. The electronic and lattice structure of a reconstructed cleaved GaAs (110) surface is shown schematically in Fig 3.1.

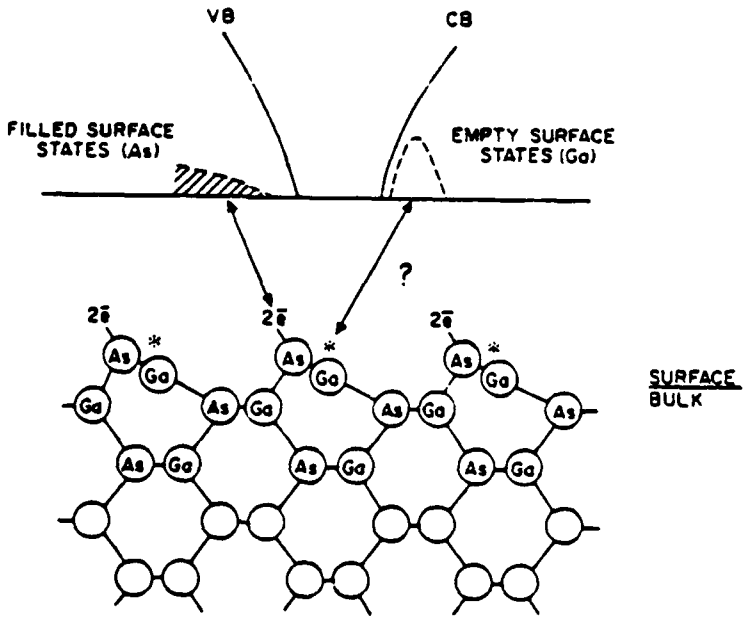

Fig. 3.1 Schematically Presentation of a Cleaved GaAs Surface (Ref 1)

This model is very different from the dangling bond model where the surface states are expected to be present near the middle of the bandgap. In Fig 3.1 the empty surface states lie above the conduction band minimum and the filled states below the valence band maximum. Thus the surface states have been swept out of the bandgap by the reconstruction of the surface atoms.

The fact that these intrinsic surface states move out of the bandgap means that on a perfect but reconstructed GaAs (110) surface there will be no pinning of the Fermi level before foreign atoms are deposited. Thus it is possible to follow the surface position of the Fermi level as foreign atoms are deposited and gain information on the effect of such depositions. This is done for a wide range of elements and reported by several authors. W. E. Speicer shows some data for Al, Ga, In and Ge on n-type and p-type GaAs in Fig 3.2.

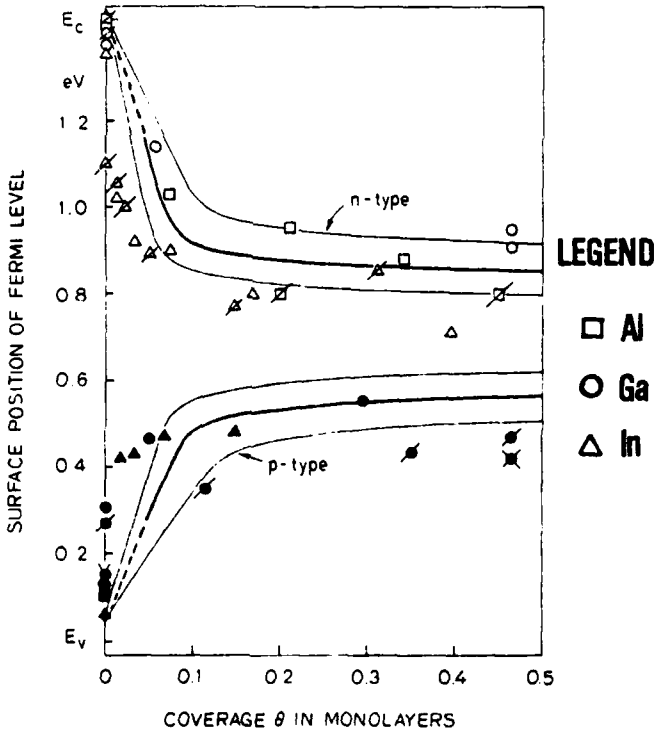

Fig. 3.2 Surface Position of the Fermi Level Versus Adatoms Coverage on the GaAs (110) Surface (Ref 1)

Note the rapid rate of Fermi level stabilization, and the similarity of the stable Fermi level position for different adatoms. The same pinning position is also found for a wide range of other materials on GaAs.

The pinning position of a number of different atoms deposited on GaAs are shown in Figure 3.3

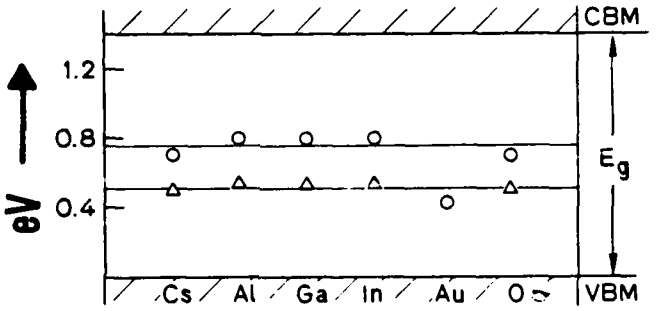

Figure 3.3 Stable Fermi Level Positions for Space Overlayers on GaAs (110) (Ref 1)

As can be seen, the pinning position is largely insensitive to the metal work function. That is believed due to a high density of electronic states at a few discrete energies at the metal-semiconductor interface. These states are determined to first order by native defects such as vacancies, antisite defects or more complex defects. It can now also be understood why GaAs semiconductor Schottky barriers depend so little on the presence of their oxide layers before depositing the metal: oxides and metals induce the same electric levels in the semiconductor (Fig 3.3).

3.2 SCHOTTKY CONTACTS

Schottky contacts are used for GaAs FET's due to the fact that no useful native oxide may be formed as for Si MOS transistors.

A Schottky barrier results when a metal is placed in intimate contact with a semiconductor such as GaAs, the barrier has the electrical characteristics of a diode.

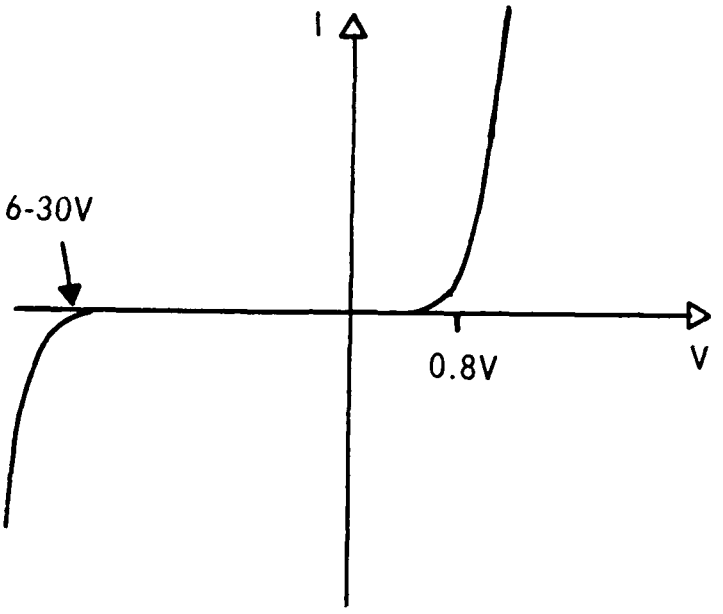

Fig 3.4 Schottky Contact IV Characteristic

The region underneath the metal is depleted of carriers and is therefore an insulator. The distance the depletion region extends into the crystal is a function of the voltage applied between the metal and the semiconductor. At high frequencies the Schottky contact is equivalent to a capacitor.

The depletion region exists even when no external voltage is applied, due to the metal work function (0.8V). If a negative voltage is applied the depletion region extends further into the semiconductor transistors. This will increase the channel resistance. If a positive voltage is applied the depth of the depletion region

decreases. If the voltage becomes too large in one of the directions, breakdown phenomena occurs and substantial currents may flow. The forward breakdown voltage is approximately 0.8V, the reverse breakdown voltage depends on the doping concentration and other factors, but generally is in the range of 6-30V.

As shown in Chapter 3.1 almost any metal placed on GaAs will yield a Schottky barrier with about the same Fermi level, (0.75eV for n-type and 0.5eV for p-type semiconductors.) When choosing metal for contacts, good adhesion and thermal stability must be taken care of. Metals meeting both criteria include Al, Cr, Ti and Mo. Of these, only Al has sufficient electrical conductivity.

Gold is often used for interconnections. However, one problem with gold is that it can diffuse through metals and initiate diffusion problems, a barrier metal between the Schottky metal and gold may solve this problem. Platinum, molybdenum and palladium have been used.

Gallium is a rapid diffuser in many metals, and such diffusion encourages similar diffusion of the metal into the GaAs degrading or destroying the diode properties of the Schottky junction.

Below are some metal combinations used for Schottky contacts listed, the first metal is nearest the substrate.

Metal Combm.	Device	Comments
Al	Analog gate	Problem interfacing gold
Ti Pt Au	Analog gate	Highly reliable
Ti Pd Au		Ti thickness 1000-2000 A^{o}
Ti Mo Au		
Cr Pd Au		Au thickness 5000A^{o}
Mo Al		
Ti W	Digital FET	

3.3 OHMIC CONTACTS

A contact is ohmic if the I-V characteristic is linear or near linear.

The unified defect model shows that there is a high density of interface states near midgap, and that approximately the same barrier height is observed on n-type GaAs regardless of the metal used. This suggests that for ohmic contacts to GaAs the Fermi-level is pinned near midgap as shown in Fig 3.2. For charges to tunnel through the resulting high Schottky barrier present at n-type GaAs ohmic contacts the GaAs must be heavily doped. In practice n^+GaAs layers are fabricated at the metal to n-GaAs interface to enhance tunneling. Unfortunately, the necessary doping level for GaAs is at least 10^{19} atoms/cm^3, these doping levels are not easily achieved by any growth or doping techniques unless by MBE.

The most common approach to fabricate ohmic contact on GaAs is to apply an appropriate metallization in the desired pattern and then alloy the metal into the GaAs. During this process a component of the metallization enters into the GaAs and highly dopes the surface layer. Possible dopants for n-type material are Si, Ge, Sn, Se, and Te, for p-type material Zn, Cd, Be and Mg. When heated the metal alloy usually melts first, as the temperature increases a liquid eutectic mixture of the metal and the semiconductor forms. Upon cooling an epitaxial regrowth of the semiconductor material takes place with dopant atoms from the metal alloy now substituting some of the Ga atoms on their lattice sites.

For GaAs the most used contact metallization is gold based alloys. Ge has been the most used dopant and is added to gold to form an eutectic alloy (88% Au, 12% Ge by weight), this eutectic melts at 360°C. Nickel is used as an addition to the alloy or used as a nickel overlayer deposited on top of it. The exact function of nickel seems to be somewhat debatable, but the original intent was to act as a wetting agent and prevent AuGe metal from forming balls on the surface during alloying. Approximately 280A° of nickel is used for every 1000A° of AuGe. The exact total

thickness of AuGeNi is not critical, 1000A° to 2500A° is reported. The order of application of the layers does not seem critical, Nickel could be applied first, then the AuGe. The desired alloying temperature is in the range of 450-500°C. The contact alloying step is usually performed in vacuum or in an inert atmosphere. A description of the alloying process is given by R. E. Williams in Ref 2.

Contact resistivities have been found to improve as the thickness of the gold capping layer increases. Hence, the use of a top, capping layer of gold can improve contact resistance. However, it is also possible that too much gold could getter more gallium than there is germanium available to replace it. If this occurs, the resulting gallium vacancies can cause a high resistance region. The use of a barrier layer, such as Ti-W, placed between the AuGeNi and the extra gold has been suggested to prevent this effect. Obviously, the exact situation is complex. In practice, an extra gold layer does not seem to degrade contact resistance for gold thicknesses in the range of 0.3 to 0.5 um."

REFERENCES

3.1 William E. Speicher, Stephen J. Englast, The Unified Defect Model and its Application to GaAs Integrated Circuits, VLSI Electronics Microstructure Science, Vol 10, Academic Press Inc, 1985.

4.0 MICROWAVE TRANSISTORS

Little success has been achieved in making high performance bipolar transistors in GaAs, as the minority carrier lifetime is very short (10^{-85}), in Si the lifetime is more than five orders of magnitude longer ($2.5X10^{-35}$). The minority carrier lifetime is directly related to the transistors performance since the number of carriers which reach the collector depends on how many have recombined with majority carriers in the base region. The loss of minority carriers can be compensated for in part by reducing the base width, but the device fabrication then becomes more difficult.

The performance of field effect transistors (FET's) depends on majority carriers, the mobility of electrons in GaAs is over five times the mobility in Si. N-channel FET's fabricated on GaAs therefore have substantially higher performance than n-channel FET's on Si. P-channel FET's on GaAs on the other hand offer no speed advantage over Si due to the fact that the hole mobility is lower than that of holes in Si.

The most common FET device used in Si, the metal oxide semiconductor (MOS) is not easily made in GaAs as this material does not have a high quality native oxide. Best suited to take advantage of the high electron drift velocity in GaAs is the metal semiconductor field effect transistor (MESFET) using Schottky gates. The junction field effect transistor is used, but this device is usually slower than its MESFET counterpart.

MESFETS are used both in low-noise and power microwave circuits. The introduction of planar GaAs technology based on selective ion implantation made possible the fabrication of more than one device type during the same process, and made it possible to fabricate GaAs logic devices.

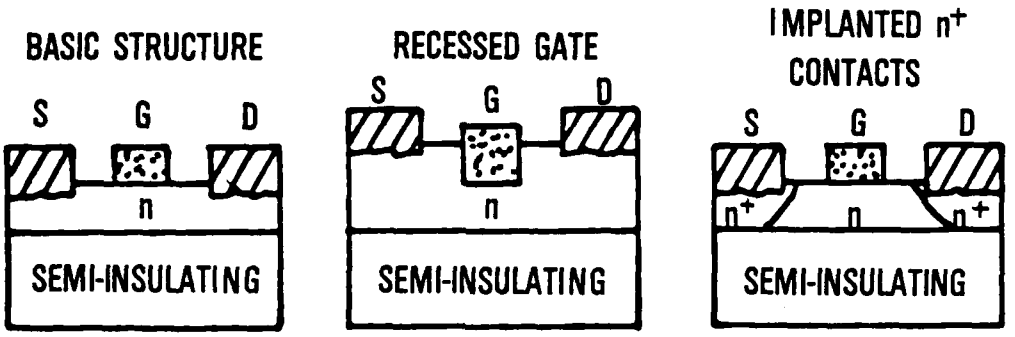

Figure 4.1 Variations of the Basic MESFET

Figure 4.1 shows variations of the basic MESFET structure. Ohmic contacts are used for drain and source, and Schottky junction for gate. The active n-layer may be formed by epitaxial growth or by ion implantation into the substrate.

EQUIVALENT CIRCUIT

The conventional equivalent electrical circuit based on the model of Shockley is only a first order approximation to the GaAs MESFET transistor. By introducing constant series resistances as indicated in Figure 4.2 a better fit to experimental measurements may be obtained.

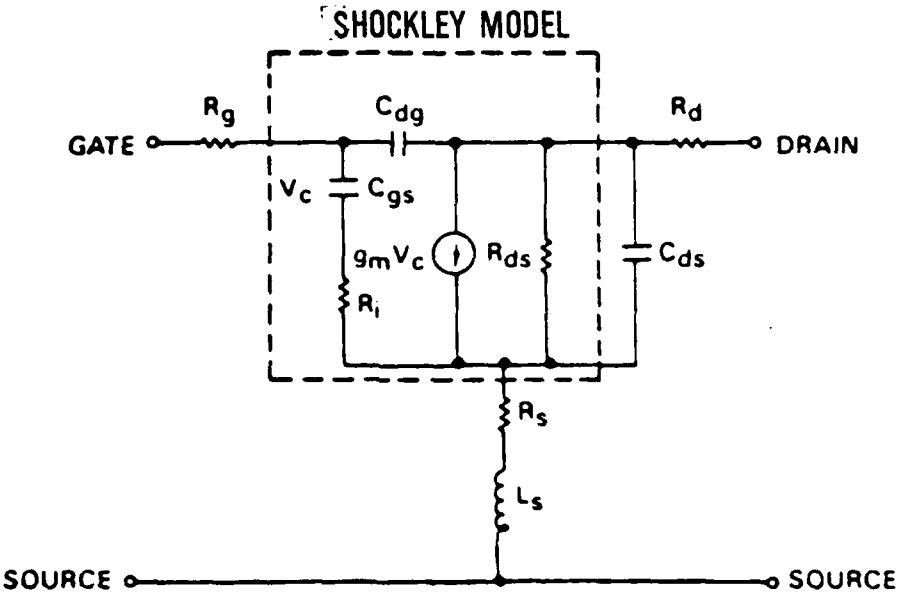

Figure 4.2 Equivalent Electrical Circuit

The surface Fermi level ot GaAs is pinned by a high density of surface states, the surface potential of a free surface is therefore approximately the same as that of a Shottky metal gate at zero bias. This forces the depletion layer to extend toward the semi-insulating substrate not only underneath the gate electrode but also under the free surface between source and gate as well as between gate and drain as shown in Figure 4.3A. Forming of free As on the surface, as reported by several authors, during high temperature treatment may also interface the same way.

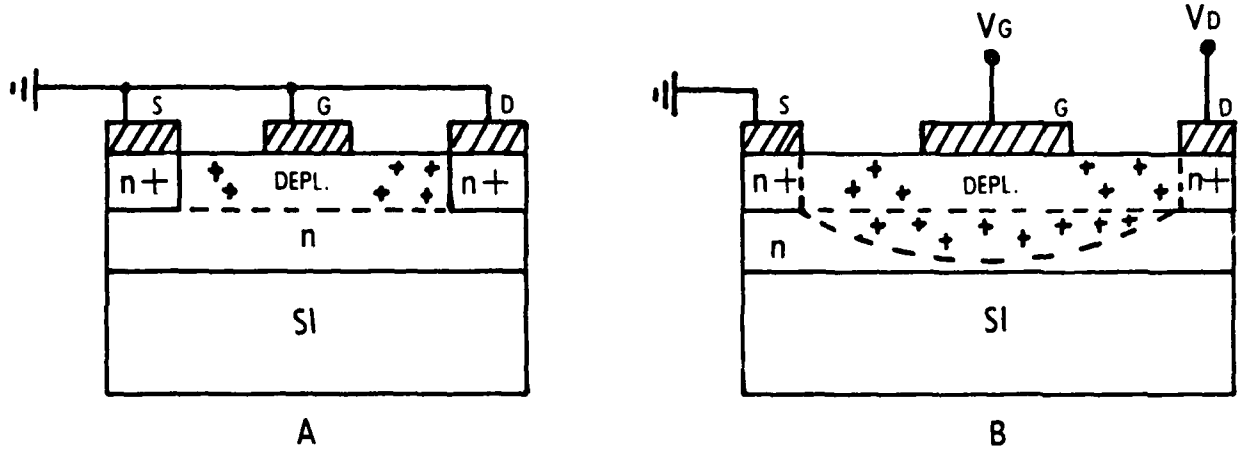

Fig 4.3 Schematic Representation of the Surface State Effect in a MESFET

The depth of the depletion is determined by the electrical field strength between the surface and the conducting channel. If we for a moment suppose the surface to have a finite and homogeneous sheet resistance, the voltage between the gate and the source as well as between the gate and the drain will vary linearly along the surface when biased, the depletion layer will then take a shape shown in Figure 4.3B. By using this model we assume that the total depletion layer between source and drain is modulated by the gate voltage, not only the portion underneath the gate. The existence of a non-zero conducting skin at or near the surface is reported by several authors S.R. Blight et al (Ref 4.2) used Deep Level Transient Spectroscopy (DLTS) to investigate the physical mechanisms of the commonly observed drift, hysteresis and transient anomalies of GaAs current-voltage characteristics. They demonstrated that "hole trap" signatures originated not from changes in the hole trap population in the channel active layer-substrate interface but from changes in

occupation of surface states in the source-gate and gate-drain access regions of the device. The work of T. Hariu et al (Ref 4.1) gives a new electrical model of GaAs MESFET's based on this effect, where variable series resistances and variable gate capacitance is added to the intrinsic FET model.

Long term drift in GaAs MESFET drain bias current and consequently gain and noise figure changes after voltage turn on has been a problem (Dumas et al Ref 4.9). The drift may go on for several minutes before it eventually stabilizes. H. Itoh et al (Ref 4.4) found that the drift was due mainly to surface conditions of the active epitaxial layer and only partially to deep traps at the interface between the substrate and the active epitaxial layer. H. Itoh et al indicate that the drift mechanism is a surface depletion layer between the gate and drain as well as between gate and source due to the high surface state density. When the gate is negatively biased, some negative charge at the surface, probably mobile ions or electrons trapped at the surface states, move toward the drain electrode due to a strong electrical field. Therefore, the depletion region also expands toward the drain side and the drain current decreases.

It has been shown that the drain current drift can be eliminated by appropriate surface cleaning and passivation. The phenomena may be a potential reliability problem for poor quality devices.

4.3 ELECTRICAL STRESSES IN MESFETS

The output power of a MESFET is determined by the maximum current the device can pass and the maximum voltage it can tolerate. Figure 4.4 shows a typical current-voltage characteristic for a FET transistor with a load line for maximum output power.

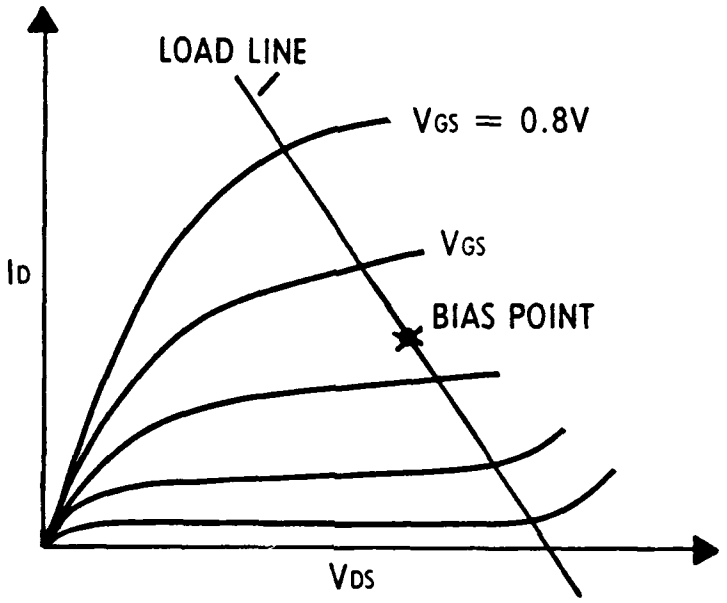

Figure 4.4 Drain Characteristic of a FET

The current is limited by the gate conductance and the voltage by the voltage breakdown of the device. Maximum power output is achieved when the gate is biased at the mid point of the load line. When the input microwave power is increased the output power increases proportionately until it approaches a fixed value, before that the output waveform starts to be distorted. By monitoring the gate DC-current, some insight into the nature of the power saturation can be gained. As power saturation is approached, a gate current begins to flow in the reverse direction due to the positive period of the RF signal driving the gate into forward conduction. At a somewhat higher input power level, the gate current changes direction, this is due to

the reverse-breakdown, effect which override the gate forward conducting current.

4.4 SURFACE EFFECTS

One of the large differences between GaAs and Si is the quality of their native oxides. Oxidation of Si surfaces is a well understood process and yields high quality well controlled layers used in device fabrication. Oxides of GaAs may easily be formed, even at room temperature a thin ($10A^{o}$) layer of roughly equal parts Ga_2O_3 and As_2O_3 is formed, but it is not stable.

C.D. Thurmond et al. (Ref 4.13) has investigated the equilibrium phase-diagram of Ga-As-O. Their experiments and calculations have demonstrated that the only stable phases that can exist in thermodynamic equilibrium with GaAs are Ga_2O_3 and elemental arsenic. Any As_2O_3 will react with GaAs according to the equation

$$As_2O_3 + 2GaAs = Ga_2O_3 + 4As.$$

This reaction occurs spontaneously at high temperature, at room temperature the reaction is going on but slowly. On a GaAs crystal surface exposed to air native oxides will slowly form, and fractions of a monolayer of free As should be expected.

During high temperature processing, such as annealing ($860^{o}C$), diffusion and alloying ($500\text{-}600^{o}C$), for a long time, a complete conversion of any As_2O_3 to free As may occur. The use of dielectric capping layers that incorporate oxygen, e.g. SiO_2 or oxygen-contaminated Si_3N_4, may supply oxygen for buildup of As_2O_3, thus increasing the amount of arsenic produced during high temperature processing.

A monolayer of free As is sufficient to increase drastically the surface recombination velocity and surface leakage current due to midgap states and may lead to long term device failures or changes in electrical parameters as leakage currents.

The As layer thickness and continuity depends on the surface treatment, temperature and capping material, the possibility that a conducting layer may form on the surface is a reliability risk.

4.5 LONG TERM BURNOUT

Burnout during DC-bias aging or during actual operation is a serious reliability hazard. This type of failure may occur without overstressing the device and is of time dependent nature. There has not been reported any electrical precursor for long term burnout, but several authors report white light emmision along the gate side of the drain contact or the n+ ledge prior to burnout. S.H. Wemple (Ref 4.15) reports that during high temperature aging tests to study this phenomena, they observed localized white-light emission along the gate side of the n+ ledge, these light spots were entirely absent prior to aging and developed approximately after 3 min at 350°C case temperature. Reducing the temperature to 250°C yielded essentially the same results except that the time required to develop the light was substantially longer. Their key observation was that burnout always seemed to occur after light formation and that those devices which exhibited short (long) light formation times had short (long) burnout time. Aging experiments at 190°C ambient showed light development after 120 hours with burnout after 145 hours. By stripping the SiO_2 passivation layer and following with a very light surface etch, it was shown that the etching treatment, which removed the natural oxides and 100A° of GaAs, eliminated the n+ light spots which had developed during aging. Stripping the SiO_2 alone had no effect. This and similar data strongly implicate the GaAs surface in the long-term burnout process (Ref 4.16 and 4.18).

White light emission in GaAs generally involves radiative electron hole pair recombination, the driving force is field-enhanced impact ionization. The magnitude of electrical fields must be larger than 3×10^5 V/cm Localized melting of GaAs in the light emitting spots is also reported.

During normal operation a large electric field forms at the gate edge. If a conductive layer of free As is formed on the surface, the field pattern may easily be disturbed and local high field domains may form between the gate and drain, ultimately creating very high electrical fields at the drain edge followed by burnout the same way as for the instantaneous failure mode.

4.5.1 GATE-DRAIN BREAKDOWN, SURFACE EFFECTS

Figure 4.5 shows results of numerical simulations on a somewhat unrealistic transistor model with no surface flaws made by W.R. Frensley (Ref 4.5) with the goal to understand the nature of the power limiting breakdown phenomena. Figures 4.5A and B show the siutation when the gate is biased at V_G=0.0V and the drain is at 4V. Gate depletion is apparent in the electron density plot, the electrical field is strongest at the gate edge. Figures 4.5C and D shows the situation when the gate voltage V_G= -2.8V and the drain voltage V_D = 15V. The channel is pinched off and there is a very large electrical field at the gate edge. The field shown corresponds to the situation when avalanche between gate and drain just starts. The breakdown seems to start at the gate edge, experimentally this was verified by the observation of light emission from this region under power saturated microwave operation by W.R. Frensley..

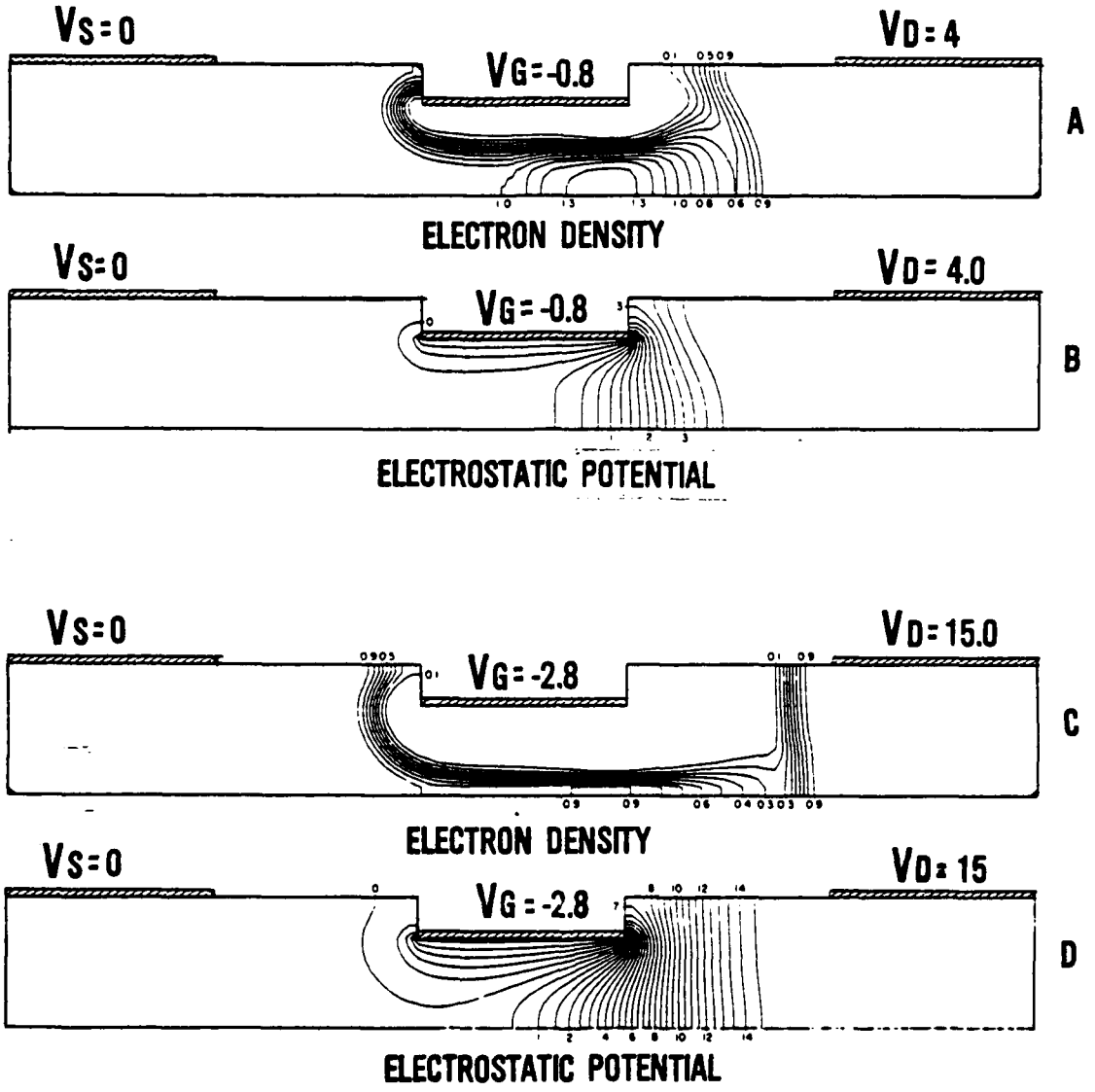

Figure 4.5 Results of Numerical simulation of a Recessed FET Structure

A: Electron Density-Plot V_g=0.0V.

B: Electrostatic Potential.

C: Electron Density at Breakdown.

D: Electrostatic Potential at Breakdown.

M.P. Zaitlin (Ref 4.6) has used a numerical technique for calculating the reverse breakdown voltage V_{BR} and used that for investigating the effects of a gate recess and a n+ layer, as shown in Figure 4.6. This geometry is usually introduced in order to reduce the parametric resistances.

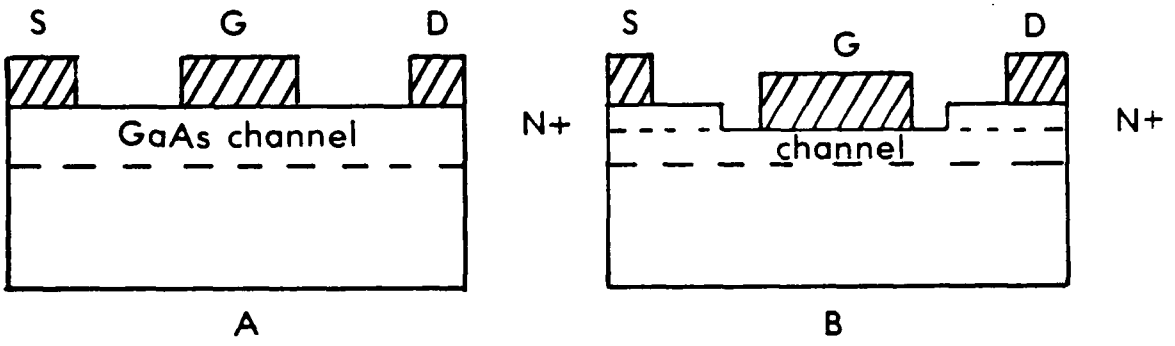

Figure 4.6 (A) Geometry for Planar FET and (B) FET With n^+ and Recess

He shows that this is done in expense of the breakdown voltage. Bringing the highly conductive n+ layer in close to the gate effectively brings the gate and drain closer together resulting in larger electric fields and lower breakdown voltage V_{BR}. This effect is particulary large for thin channels that normally have the advantage of lateral spreading of the field.

The n+ layer should be more than a few tenths of a micrometer away from the gate edge and even further for thin channels. If this caution is observed, he concludes that thin channels with doping levels in the mid and upper 10^{17}'s can have breakdown voltages similar to or greater than that of more lowly doped channels

while maintaining the same current levels.

Gate-drain breakdown due to high electrical fields at the drain side of the gate may occur during manual tuning of a RF amplifier, if the gate bias voltage for some reason is drifting negatively or maybe if the input voltage swing is too large.

J.M. Dumas et al (Ref 4.9) has reported that GaAs power FETs submitted to biased life tests show gradual degradation of output power and changes in DC characteristics such as gate-to-drain breakdown voltage and gate leakage current. The life test program included some 120 power FETs with an unprotected VPE active layer. The degradation took place at 150°C channel temperature and was bias-dependent. After 200 hours when biased at pinch-off voltage, or after 2000 hours when RF operated a 25% max decrease on the output power was observed. At the same time, the gate to drain breakdown voltage decreased typically from 14V to 8.5V for reverse biasing tests and from 14V to 10V for RF-operation. During RF operating white light was observed between gate and drain and along the gate edge. They conclude that the long-term degradations observed are due to the development of a surface conductive layer between gate and drain reducing the breakdown voltage and the output power. They suggested that the release of elemental metallic arsenic from As_2O_3 during processing and aging might be the reason for the conductive layer.

4.5.2 Gate Degradation Mechanisms

The stability of the gate contact on GaAs devices at normal operating conditions is imperative for the performance and the reliability of these devices. Three different failure modes have been reported.

1. Electromigration due to high current
2. Interelectrode material migration due to high electric fields
3. Interdiffusive effects at the metal-GaAs transition

4.5.2.1 ELECTROMIGRATION DUE TO HIGH CURRENT

This failure mode is the same as found in metal lines in Si components and is not discussed here.

4.5.2.2 INTERELECTRODE MATERIAL MIGRATION

Lateral material migration across the GaAs surface between neighboring electrodes may lead to interelectrode bridging and eventually short the electrodes. This migration is due to the high electrical fields between the electrodes, and has been more pronounced in recent years as the power FET's voltages have been increased by special processing such as introducing n+ layers and recessed gates. High RF-power pulses may also lead to metal migration.

Several authors have reported that electrical field induced migration of electrode material strongly depends on surface treatment.

Kretschmer and Hartnagel (Ref 4.7 and 4.8) have studied interelectrode material transport in unpassivated and in PECVD-Si_3N_4- passivated GaAs planar structures using x-Ray-Photoelectron Spectroscopy (XPS). The failure mode associated with interelectrode material transport is bridging followed by massive damage of the device. They found that the stability of metal contacts and dielectric layers on GaAs is strongly affected by the GaAs surface which when treated by various etching and cleaning solutions shows a strong correlation between migration and the amount of arsenic oxide (As_2O_3) and elemental As on the surface. Arsenic- and gallium-oxides are formed on the surface of GaAs during high temperature processing steps. Oxygen may be supplied from SiO_2 or poor quality SiN passivation or capping layers. Arsenic oxide on the surface will then supply elemental As by a reaction with GaAs. The amount of free As is a function of time, temperature and the amount of As_2O_3.

Kretschmer and Hartnagel give the following conclusion of their study:

- Samples cleaned by organic solvents only, exhibit primarily Ga- and As-oxides.
- Surfaces treated by acid etchant (H_2SO_3) exhibit a strong contribution of arsenic oxide even down to a depth of the order of 25A^o, a reduction of threshold voltage up to 50% has been observed.
- The treatment with basic etchants removes both As- and Ga- oxides and hence results in an approximately stoichiometric Ga to As ratio. The threshold voltages are more than 35% higher than the values for the non-etch surfaces.

Anderson et al (Ref 4.10) has reported a study of high power FETs under high power gate pulses to simulate the radar environment of transceivers which share the same antenna. They found a gradual degradation of DC and RF-characteristics before massive damage occurred. Metal migration appeared to be the cause in Al-gate devices, the migration started particularly from irregularities along the gate. The metal bridging appeared to be different with TiW gates as there were less locations where metal migration occured, but a depression typically formed between the gate and source. TiW may be a high reliability metallization for MESFET's used in high power pulsing because the metal migration appears to be reduced.

4.5.3 INTERDIFFUSION EFFECTS AT THE METAL-GaAs TRANSITION, VERTICAL ELECTROMIGRATION

Accelerated stress tests on microwave power GaAs MESFET's done by Kashiwagi et al (Ref 4.11) under RF operation at 8 Ghz with temperatures between 210°C and 250°C identified void formation in the gate electrodes. The devices tested consisted of 0.8 um aluminum gates fabricated using self-aligned gate technology. They concluded that:

(1) Aluminum from gate fingers diffused microscopically into GaAs, probably by electric field or current. This aluminum diffusion caused voids in most gate fingers.

(2) Schottky diode characteristics were locally lost where this aluminum diffusion proceeded most rapidly.

(3) Gate current concentrates at this location and finally results in catastrophic burn-out by gate current itself, or by hot spots caused by nonuniform gate bias.

J. Wurfl and H.L. Hartnagel (Ref 4.12) have studied Schottky Al and Ti-Pt-Au contacts on GaAs by stress testing under bias at room temperature and up to 250°C. The influence of these stress tests on the interface properties were studied by XPS sputter profiling and correlated with electrical measurements. Regarding Al contacts they concluded:

Thermal stressing of Al-GaAs Schottky contacts increases the barrier height.

The shape of the I/V characteristic is found to be strongly influenced by GaAs surface treatment before Al metallization and on the bias condition.

Stress conditions and GaAs surface treatment affect the Ga to As ratio at the interface. This ratio is shown to be strongly correlated with the interface oxygen content. It was found that a field-assisted aluminum diffusion took place along grain boundaries even at room temperatures. Ti-Pt-Au contacts were stable at room

temperature over a period of 200 hours, but at 300°C a Ga diffusion into Ti and a subsequent Ti diffusion into Ga vacancies took place.

Reliability problems may arise with Al metallization on GaAs even at room temperature if the oxygen concentration at the Al-GaAs transition is not kept low during device fabrication. Both Al and Ti-Pt-Au failed during this study at elevated temperatures due to metal diffusion into GaAs and Ga diffusion into the metal. A diffusion barrier seems necessary for reliable operation at elevated temperatures.

4.6 INSTANTANEOUS BURN-OUT

The primary weakness of planar GaAs microwave transistors are the low gate-drain avalanche breakdown voltage which limit the power handling capability. The primary failure mode is breakdown at the gate side of the drain metallization. By observing the drain current/drain-source voltage (Id/Vds) characteristics of transistors while increasing Vds a sharp turnaround point can be observed when the MESFET breaks down. This Critical voltage shifts to higher values with decreasing Vgs. Several authors have reported observations of visible light emission at the drain edge before avalanche breakdown occurs at the same spots. A high electrical field is necessary to produce the light. These observations, however, are inconsistent with several device electrical field simulations reported (Ref 4.5 and 4.19, Fig 4.5) which shows that the maximum electrical field always exists at the gate edge independent of the geometrical shape of the MESFET.

4.6.1 IMPROVED SIMULATION OF a MESFET

Hiroshi Mizuta and K. Yamaguchi (Ref 4.20) introduced the surface-potential effect of GaAs into a two-dimensional device simulation and have analyzed in detail the gate-drain breakdown in the surface depletion layer. Their simulation shows a drastic change in the potential distribution and thereby in the electric field pattern due to the surface effect. Their model predicts high electrical fields at the drain edge, as has been observed by experiments, Fig 4.7. The surface effect is, as

discussed before, due to a very high surface state density of GaAs and electrons captured by these states. Possible surface defects are considered to be non periodic arrangements of atoms, native oxide of Ga and free As. Thus there exists a surface depletion layer between the electrodes on GaAs MESFETs.

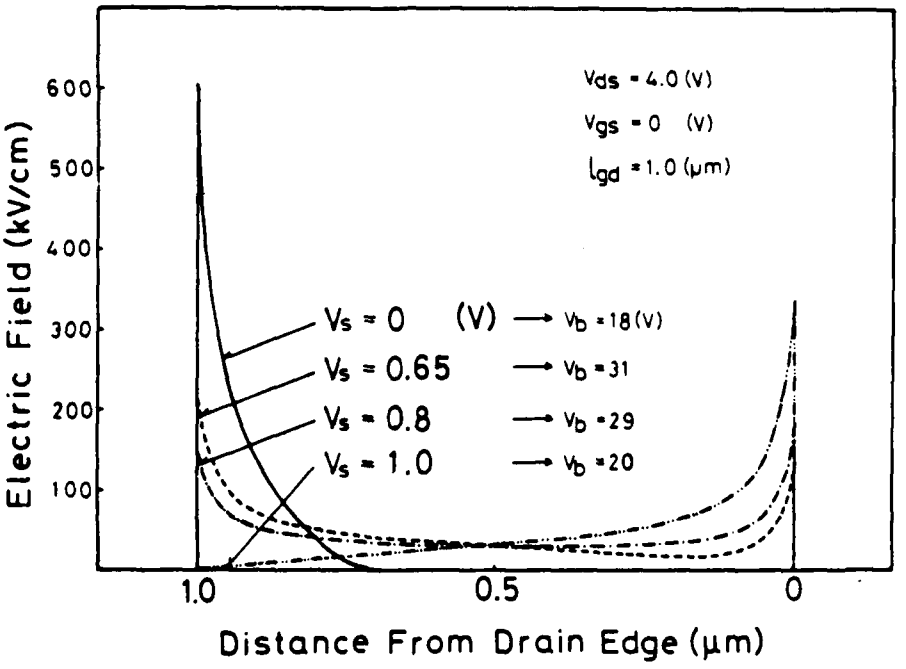

Figure 4.7 Electrical field distribution on the surface between gate and drain electrodes of planar GaAs MESFET

They also give a one-dimensional analytic model for the electrical field strength including the surface potential. Electrons captured by the surface states are assumed to be distributed uniformly on the surface between the gate and drain electrodes. Fig 4.8 shows a model for space-charge distribution on the surface.

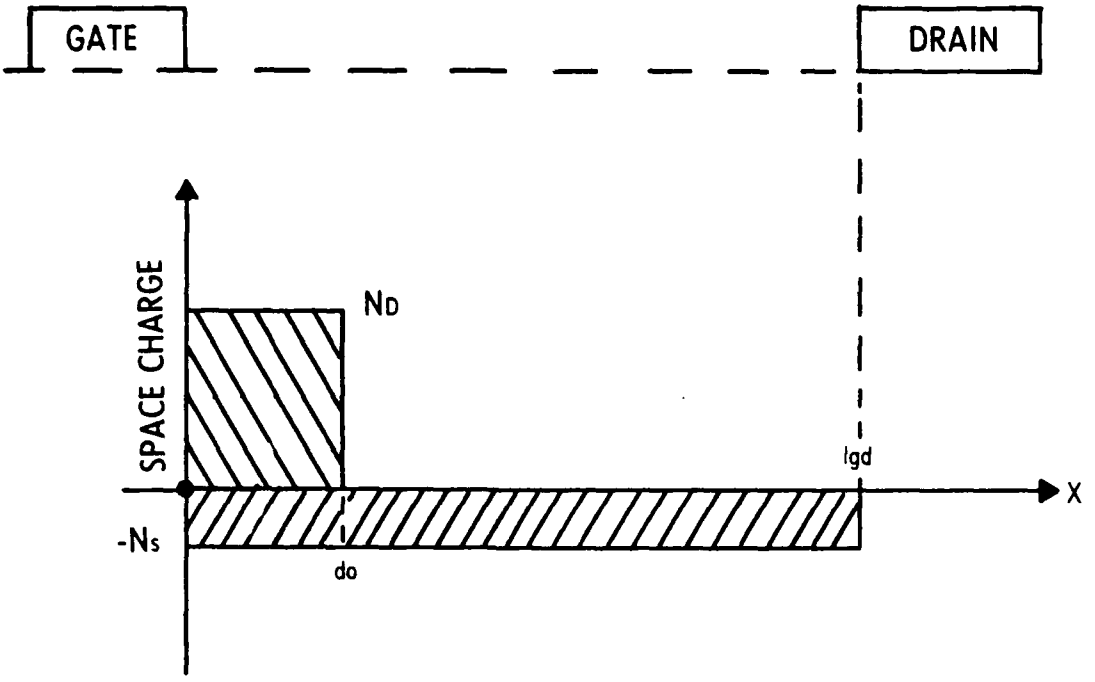

Fig 4.8 Model for Space-Change Distribution on Surface between Gate and Drain.

do = width of the depletion layer.

N_S = Surface acceptor concentration

N_D = Donor concentration in active layer

From this one can see that the electrical field at the gate edge becomes smaller when the surface charge concentration N_s increases, on the other hand, the electrical field at the drain edge E(lgd) is increasing with increasing surface charge density N_S.

This may explain the degradation of breakdown voltage of some devices. Poor process quality may produce more than normal surface states and thereby higher surface acceptor concentation N_S which results in higher electrical field at the drain

edge.

Figure 4.7 shows calculated electrical field distributions on the surface between gate and drain for various values of surface potential Vs. "As shown, the electrical field strength at the gate edge decreases and the strength at the drain edge increases with increasing Vs. A larger value of Vs represents an increase in the number of electrons captured by the surface states. The charge of these electrons cancels the positive space charge in the depletion layer of the Schottky gate and therefore weakens the electrical field strength at the gate edge. On the other hand, these electrons form a peak of the electric field strength at the drain edge. The drain breakdown voltages V_B with various V_S are also indicated in Fig 4.7. This theoretical calculation was verified by measuring the potential distribution on the surface using a Scanning Auger Microscope (SAM) by S. Tiwari et al (Ref 4.22). By experiments Mizuta and Uamaguchi found the value of V_S to be about 0.65V, which is consistent with reported values measured with photoemission spectroscopy by W.E. Speicer et al (Ref 3.1).

4.6.2 IMPROVED GEOMETRY OF MESFETS

This simulation gives valuable information for the understanding of failures in MESFETs and why certain changes in the geometry improvers the avalanche breakdown voltage.

Planar MESFETs typically have a drain to source breakdown voltage of 10V when the gate voltage is V_g=0V. At pinch off, the breakdown voltage increases to more than 20V.

By offsetting the gate to the source side, a wider spacing between the gate and drain electrodes is considered to be effective to obain a larger drain voltage. Introudcing a n^+ (($n = 2.10^{18} cm^{-3}$) layer between the active n- layer and the ohmic metallization increases burnout voltages by nearly a factor of two i.e., from the 10V range to 20V for V_g=0V. Furutsuka et al (Ref 4.21) introduced a recessed gate structure to increase the epi-thickness under the drain and source contacts which

improved the instantaneous burn-out even more. Wemple et al (Ref 4.15) has improved the breakdown voltage into the 40-50 volt range by extending the n^+ layer towards the gate and away from the drain ohmic metal edge by the ledge structure. All methods used to improve the breakdown voltage may be explained by the new simulation model to be due to rearranging the potential distribution and electric field distribution in such a way that the high field at the drain metal edge is weakened.

4.6.3 SUBSURFACE BURN-OUT

Figure 4.8 shows a picture of a burned out transistor on a digital GaAs device. The glassivation layer has opened up on two places and two GaAs particles seem to have erupted through the opening and are laying on the surface.

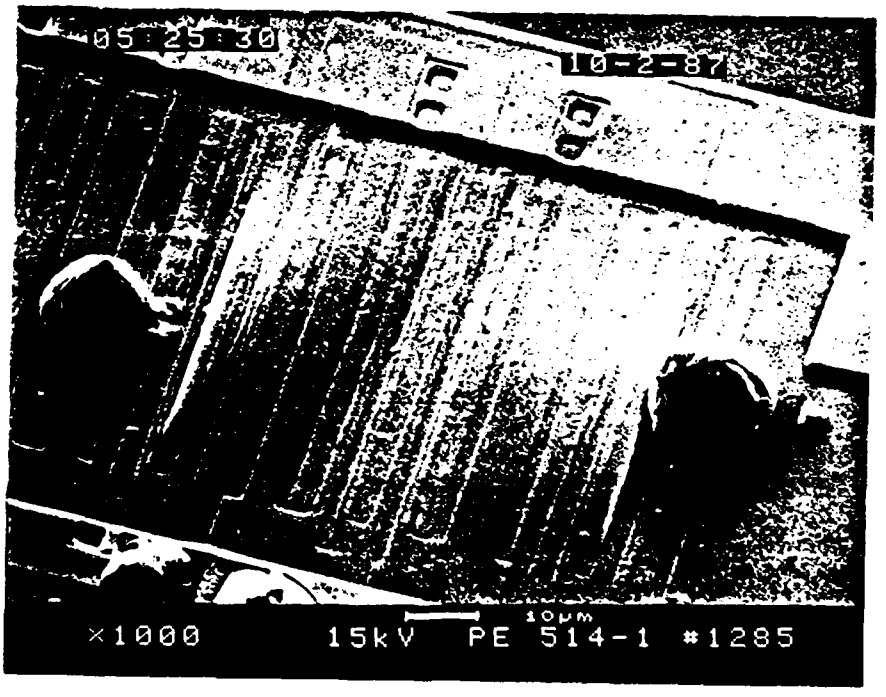

Fig 4.8 SEM Picture of a Subsurface Burn-out

Subsurface burnout is initiated by metallic filaments of low resistivity resulting from metal GaAs interdiffusion at the gate, source and drain extending deep down into the substrate. Under repeated high gate current density transient enhanced diffusion of Au through an intermediate layer into the active channel may result by the so called recoil mechanism. Repeated thermal transients at the source and drain regions under a series of high power pulses to the gate will result in a significant metal GaAs interdiffusion. This thermally-induced mechanism is well known (Ref 4.10, 4.23, 4.24) and is an accumulative process. Fig 4.9 illustrates the process.

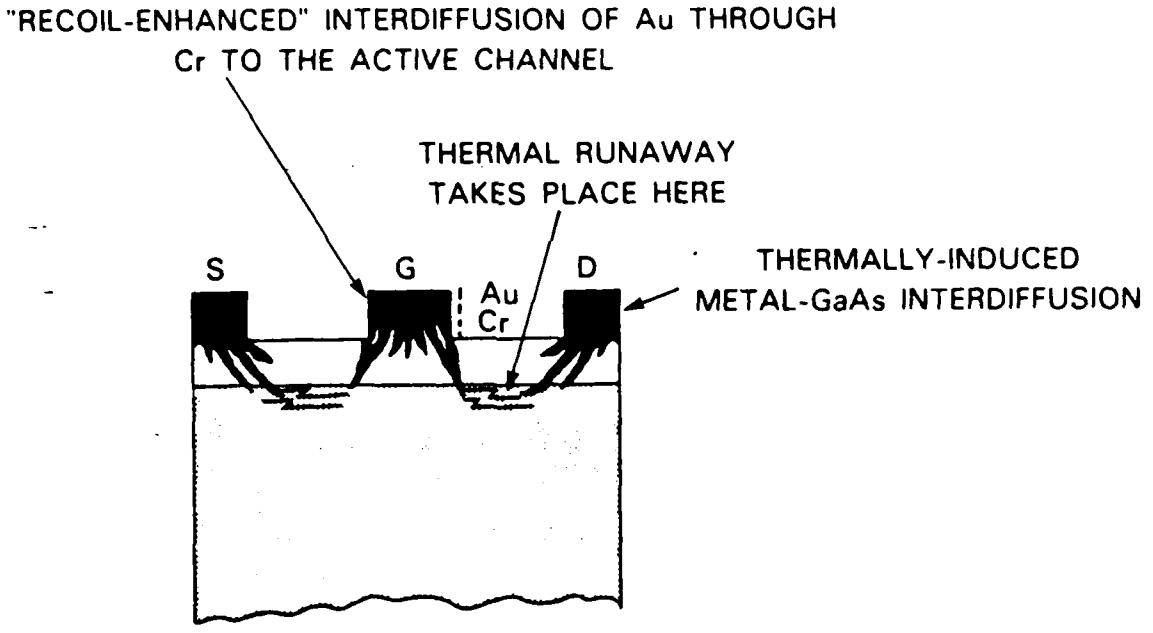

Fig 4.9 Thermal runaway is initiated when positive-temperature coefficient regions bridge two metallic filaments interdiffusing from the ohmic metallization and gate. (Ref 4.23)

The filamentary shape of the interdiffusion is believed to be due to "weak spots" in the ohmic and gate metallization. For burnout to occur, a low resistance path between filaments must be created. This can happen in the substrate to active channel interface which is a deep-level trap enriched region (DLTE). This region also has a highly postive temperature coefficient. Thermal runaway takes place in this region when heated to 500-550°C in the presence of an electric field (the intrinsic electron concentration (n_i) in GaAs at 500-550°C is $2 \times 10^{15} cm^{-3}$. This happens when this region is at or in the vicinity of the hot-electron distribution with local electron temperatures in the range of 2000°C and electron density roughly $10^{17} cm^{-3}$. During a situation as described, exponential buildup of current restricted only by outside components is possible.

The mechanisms leading to the critical runaway temperature is believed to be due to high electrical fields at the drain (3-6 KV cm^{-1}) which injects holes into the semi-insulating substrate by impact ionization and avalanche at imperfections in the drain contact. The local temperature increases as electrons recombine with holes in the substrate. Simulaton of hot electron energy densities after application of a step voltage or power pulses at the gate by Anderson et al (Ref 4.23) shows high energy density and hot electrons created near the edges of the gate and at the edge of the source and drain metallization.

Simulations by F.A. Buot (Ref 4.24) with a step gate voltage pulse applied shows about a factor of 5 decrease in energy density at the drain edge of a recessed channel FET compared with a planar FET design. With n^+ ledge geometry, burn-out powers in the 4-5W/mm range are generally observed. Some devices exhibit values which are as much as a factor of 2-3 lower. One known cause for such behavior is inadvertent localized separation (or trenching) of the N^+ ledge near the ohmic contact edge during the ion milling process used to define the thick Ti-Pt-Au ohmic contact overlay (Ref 4.15). In this case, the ledge loses its effectiveness, and burn-out reverts to its lower drain contact (planar) dominant value.

A second mechanism reported for premature burn-out is missing or lifted sections of the gate (Al) in which case the local high current density generates hot spots which induce thermal runaway.

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5.0 GaAs DIGITAL INTEGRATED CIRCUITS

The first GaAs digital circuits were fabricated on epitaxially grown active layers on semi-insulating GaAs substrates using the MESA process, Fig 5.1. With this process, selective doping is not possible and only one type, MESFET, can be made. Logical circuits were implemented using buffered or unbuffered FET logic (BFL) shown in Figure 5.1, these logic circuits require two power supplies. The power consumption is too high for VLSI application and the packaging density is low but it provides the highest speed of all GaAs logic families.

The planar GaAs process was introduced in 1978 and made possible selective doping, thus both depletion (normally on) and enhancement (normally off) transistors could be fabricated on the same die. Since the hole mobility in GaAs is lower than for Si only n-channel devices give speed gain over Si devices.

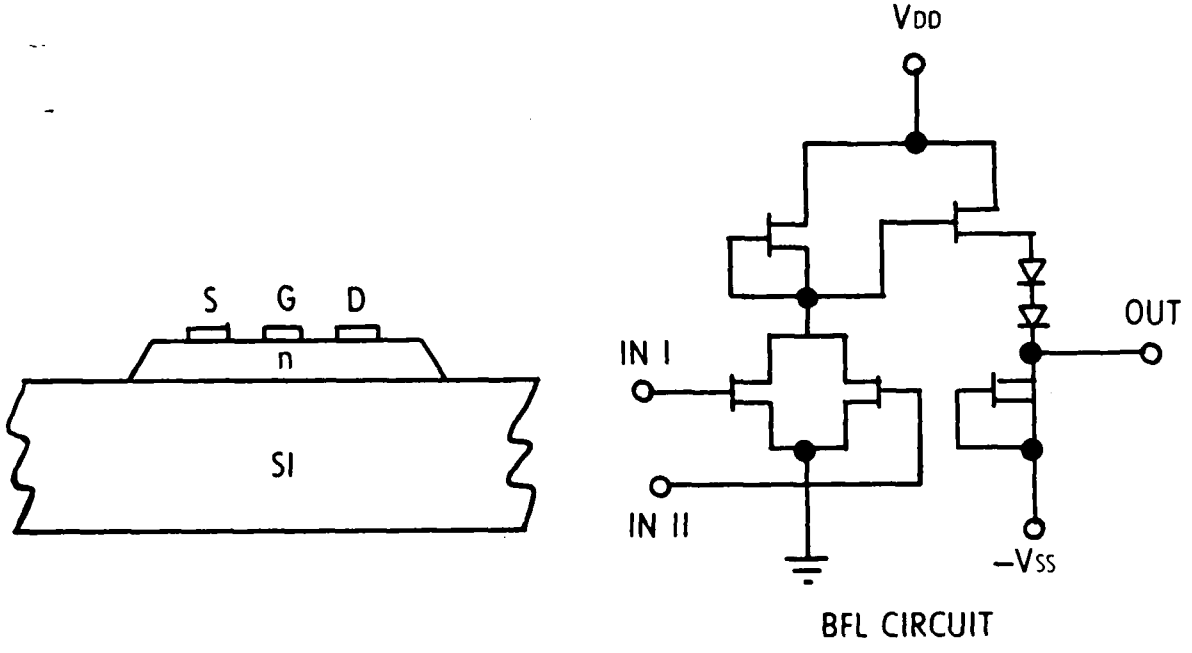

Figure 5.1 MESA Type MESFET and Buffered-FET Logic Circuit

The depletion mode FET (D-MESFET, normally on) has the largest current drive capacity per unit device width, this contributes to its high speed but also to its high power dissipation. The logic swing is determined by the pinch off and forward breakdown voltage of the gate. The pinch-off voltage can be made larger by varying the channel doping and thickness under the Schottky barrier gate. The D-FET needs two power supplies as the gate requires a negative voltage for turn off and as a consequence, any logical family based on D-MESFETs requires voltage level shifting between stages.

An enhancement mode FET (E-MESFET) is made by varying the doping level under the gate to get the pinch-off voltage to zero volt or above. The logic swing of the E-MESFET is limited to the difference between the pinch-off voltage (OV) and the forward turn on voltage of the Schottky gate (+0.5V). The MESFET consumes less power than the D-MESFET, but the noise margin is significantly lower and a stringent process control is necessary to use these transistors in LSI and VLSI components. The E-MESFET needs only one power supply.

The Schottky diode FET logic (SDFL) gate dissipates one fifth the power of the BLF gate but is about a factor of two slower. Logic gates using E-MESFET's (direct coupled FET logic, DCFL) have the lowest power consumption (50 uw/gate) but the gate delays are 2-4 times that of the BLF. Several variations of these configurations have been implemented. (Figure 5.2)

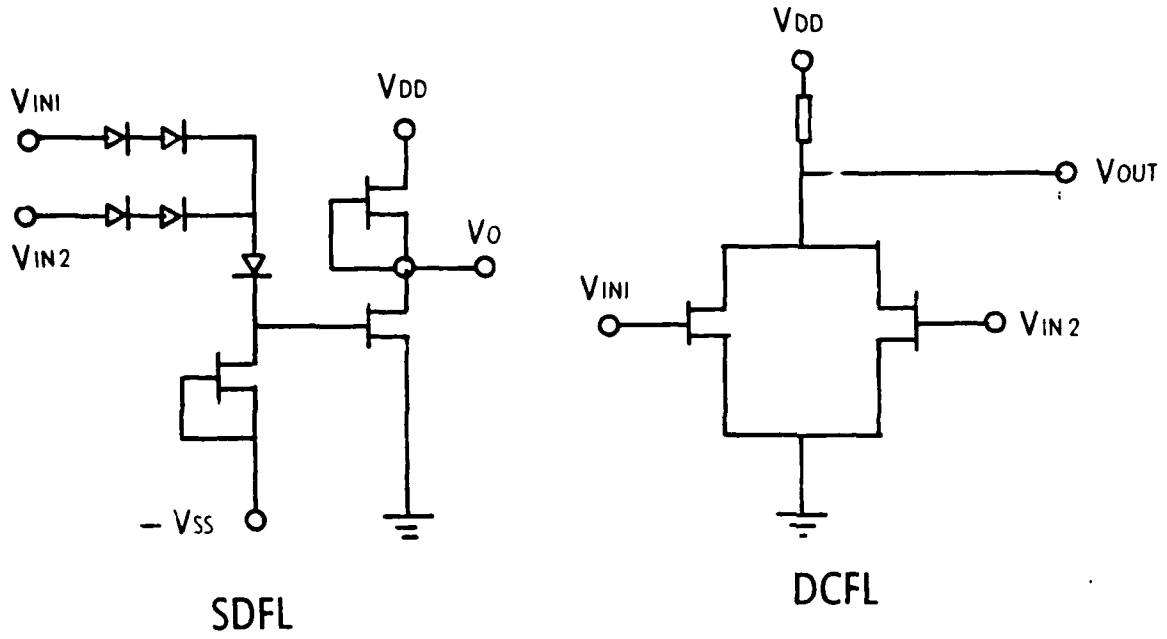

Fig 5.2 High Speed GaAs Logic Gates

5.1 GaAs PLANAR TRANSITOR STRUCTURES USED IN IC'S

Some planar transistor structures used in IC's with examples of the fabrication process are shown below.

PLANAR MESFET

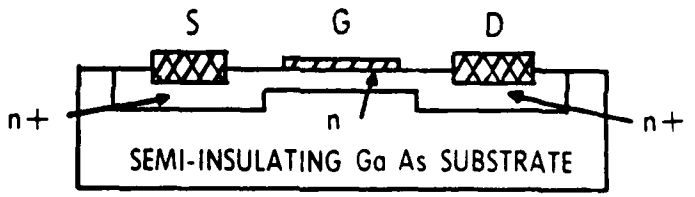

Figure 5.3 Planar Depletion MODE MESFET

The planar depletion mode MESFET (D-MESFET) shown in Figure 5.3 is fabricated by ion implantation of p-type dopants into the semi-insulating GaAs. The source and drain contacts are ohmic while the gate is a Schottky contact, typically 1 um long, the same size as the distance from source to gate and drain to gate. Any region of the source to drain channel not under the gate is conductive and precise gate alignment is not necessary. Surface quality though, has a strong influence on the transistor parameters and may influence the long term reliability of the device. Surface states and possible existence of free As on the surface may alter the electrical field in the channel outside the gate metallization and thereby altering the channel dimension. For instance, the channel resistance is modulated by the channel dimensions and the transconductance is degraded by the parasitic resistance.

$$g_m = g_{mo}/(1+R_s\, g_{mo})$$

g_m is the terminal transconductance, g_{mo} is the internal (R_s=0) transconductance and R_s is the parasitic source resistance. It's obvious that it's critical to maintain the lowest possible source resistance and keep it stable by proper cleaning and passivation of the surface. Use of self-aligned technology offers the possibility of circumventing the source resistance problem.

5.2 TRIQUENT E/D - PROCESS

The Triquent (Tektronix) E/D process shown in Figure 5.4 is typical for planar processes.

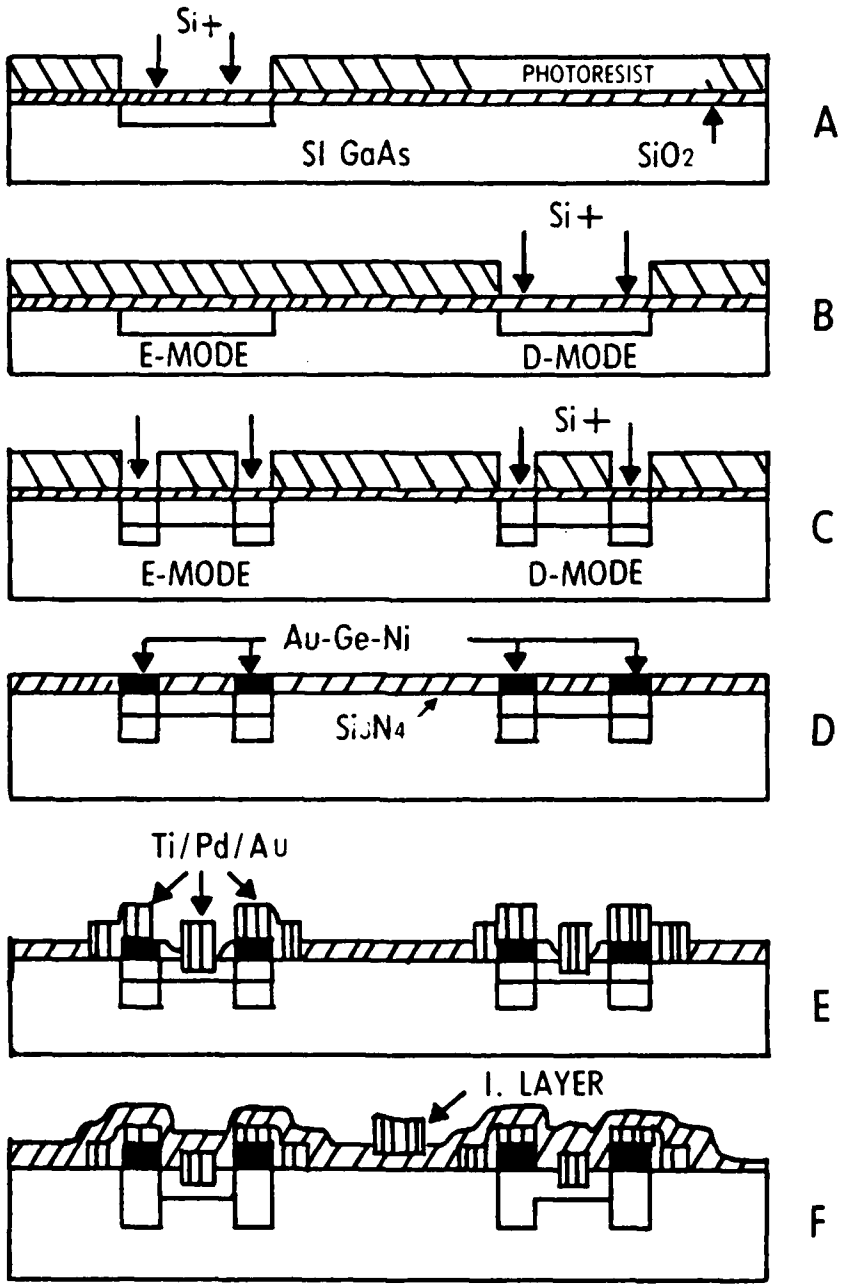

Figure 5.4 TRIQUENT (Tektronix) E/D-Process (Ref 1)

Fig 5.4a &b Active layers are created by implanting Si^+ ions through a layer of SiO_2 into the GaAs substrate, using photoresist as an implant mask E- and D-mode layers are formed by varying the implantation specification.

Fig 5.4c Using a mask with openings at source and drain areas a heavily doped n^+ layer is created deep in the crystal. The dopant concentration is kept high at the surface to make a low resistance contact possible. After implantation, the photoresist is removed and an additional layer of SiO_2 is added to act like a cap during the next step, which is annealing (activating) of the implants. These procedures go on at high temperature (860^oC), the cap is neccesary to prevent dissociation of GaAs and As out-diffusion. After annealing, the SiO_2 is stripped and the wafer coated with Si_3N_4 to passivate the surface.

Fig 5.4d The ohmic metallization Au/Ge-Ni is deposited on the n+ source and drain regions. Tektronix is using a lift off process not shown. The lift off process uses a photoresist mask with openings at the ohmic contacts. The metal is plated onto the whole surface. When the photoresist is removed, the metal remains only in the ohmic areas. This allows precise metal definitions without an etch-back procedure. The metal is thus alloyed into the n^+ GaAs forming ohmic contacts.

Fig 5.4e Tektronix is using recessed gates to give the appropriate threshold (V_T) voltage for E-MESFETs and pinch-off (V_p) voltage for D-MESFETs. Recessing reduces the parasitic source resistance by providing a thicker channel from the source to the gate region. In the active gate region, a thinner channel is needed for threshold voltage control. The process is not shown, but most probably the recess is created by chemical etching. The gate metallization is defined by a lift-off process, gate metal and metallization to the ohmic-contacts are Ti-Pd-Au.

Fig 5.4f The first layer metallization is Ti-Pd-Au defined with a liftoff process. The metal layer thickness are from substrate and up Ti: 400A°, Pd: 800A° and Au: 4000A°. The sheet resistance is about 80 m ohm/sq.

Fig 5.4g To minimize parasitic capacitance between lines. Tektronix is using the airbridge interconnecting techniques for the second level metallization.

Figure 5.5 shows a SEM picture of an actual device with air bridges.

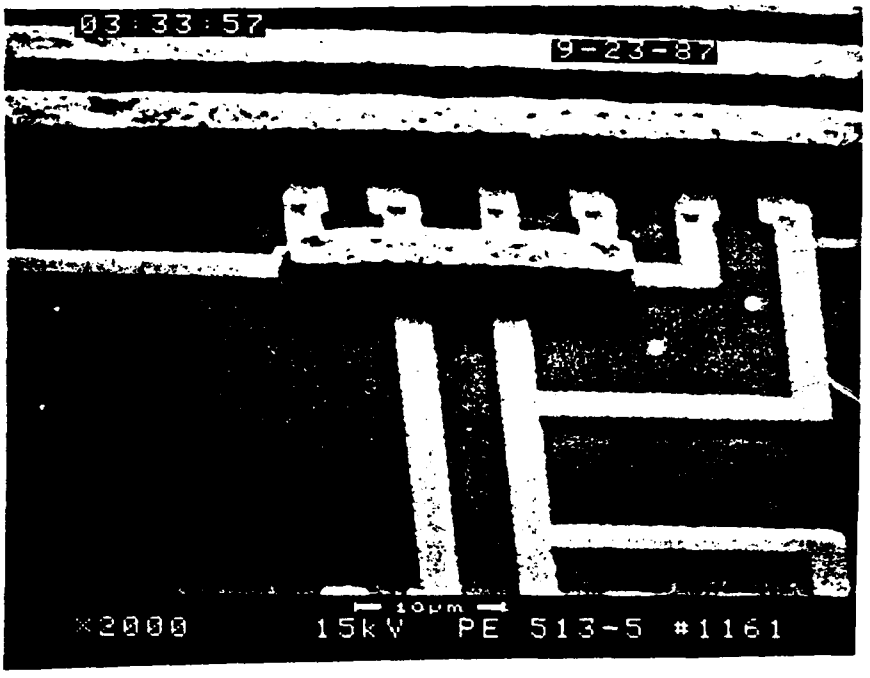

Fig 5.5 SEM Picture of a Triquent Device

The air bridge is fabricated by depositing photoresist on top of the wafer with openings for contacts and bridge support. A thin 400A° layer of Ti is sputtered on first, thereafter a thick layer of Au (20000A°) is plated. When the photoresist is washed away the air bridge is left as shown. The minimum design rules of 4 um with 7 um pitch gives an average capacitance of 7×10^{-15}F/100 um length.

After the airbridges are finished the wafer is capped with a layer of Si_3N_4. There is a total of three Si_3N_4 layers.

1. 2000A° field, Si_3N_4, sputtered
2. 2000A° interlayer, Si_3N_4, plasma
3. 2000A° glassivation Si_3N_4, plasma.

The last glassivation leaves 2000A° Si_3N_4 on top of the airbridge and a continuous 1000A° layer underneath. This capping of the airbridge adds mechanical strength to the construction.

5.3 SELF-ALIGNED GATE

Definition of the gate dimension and placement between source and drain is the most critical step in the GaAs IC fabrication process. The gate length and placement relative to the source and drain contact controls the performance of the FET. Self-aligned gate technology provides a very precise definition of the gate relative to the ohmic contacts. One such technology, called self-aligned implantation for n^+ layer technology (SAINT), is described by Yamasaki et al (Ref 2). It is illustrated in Figure 5.6.

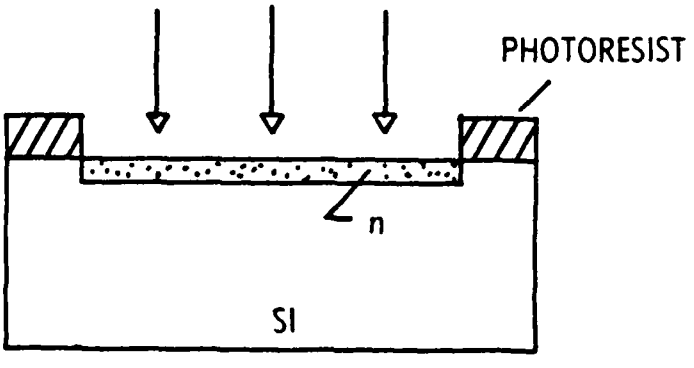

Figure 5.6A Step 1

Step 1: The channel region is formed by Si ion implantation. The photo resist is then removed and the surface covered by a 0.15-um (plasma - enhanced CVD) Si_3N_4 film.

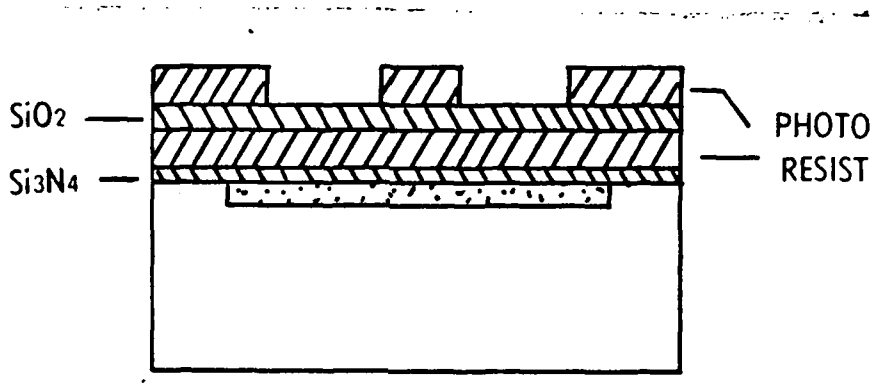

Figure 5.6B Step 2

Step 2: The multilayer photoresist film shown are selectively etched to form the undercut implantation mask illustrated in the next step.

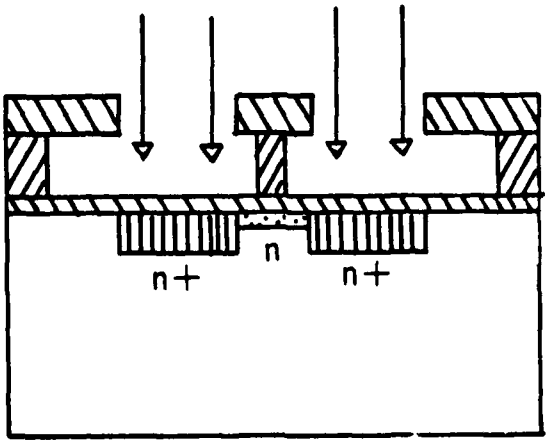

Figure 5.6C Step 3

Step 3: Si is implanted to form n^+ source drain regions. After implantation SiO_2 is deposited using RF-magnetron sputtering and the structure in the next step is formed by a liftoff process.

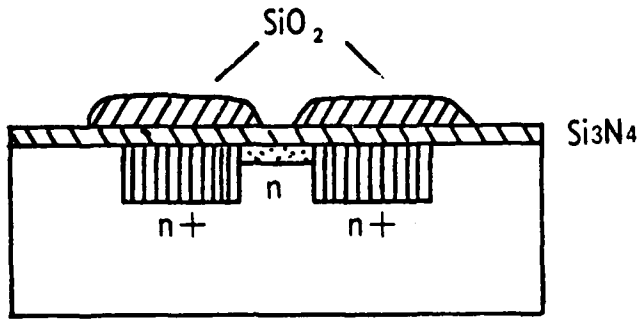

Figure 5.6D Step 4

Step 4: The implanted impurity is thermally activated at 850°C, source and drain contact holes in the passivation opened, and ohmic contacts formed by deposition of AuGe-Pt and sintering at 460°C. The gate area is then opened and the Ti/Pt/Au gate metallization deposited. Both gate and ohmic contacts are delineated by a photoresist liftoff process.

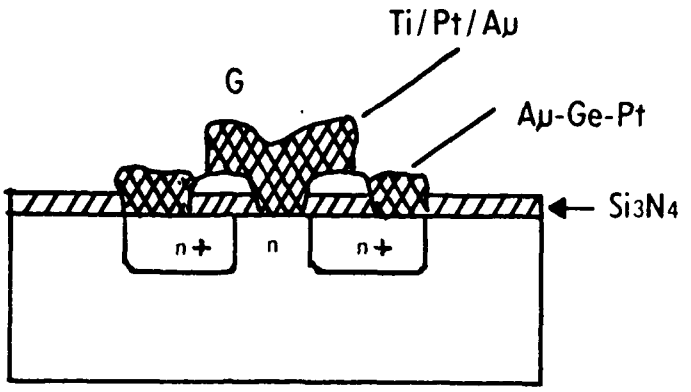

Figure 5.6E Step 5

Step 5: The distance between the gate edge and the n^+ regions is controlled by the mask shown in Step 2. This distance is a compromise betwen the series reistance and overlap capacitance between the gate and the heavily doped regions.

The self-aligned gate technology improves the performance of the devices. For instance, Greiling and Krumm (Ref 4, Fig 26) report an increase in transconductance by a factor of 18 and the current at maximum forward voltage by a factor of 11 above planar technology.

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